ABSTRACT

A delay-locked-loop (DLL) that has increased precision and a wide range of operation is formed by utilizing a chain of delay blocks to add or subtract a discreet amount of delay, and a voltage-controlled delay line (VCDL) to add or subtract a smaller amount of delay. The delay blocks allow the delayed clock signal to get close to the reference clock signal, while the VCDL allows the delayed clock signal to lock onto the reference clock signal.